PATENT ABSTRACTS OF JAPAN

(11)Publication number : 06-029525
(43)Date of publication of application : 04.02.1994

(51)Int.Cl. H01L 29/784
H01L 21/336

(21)Application number : 04-178713
(22)Date of filing : 07.07.1992

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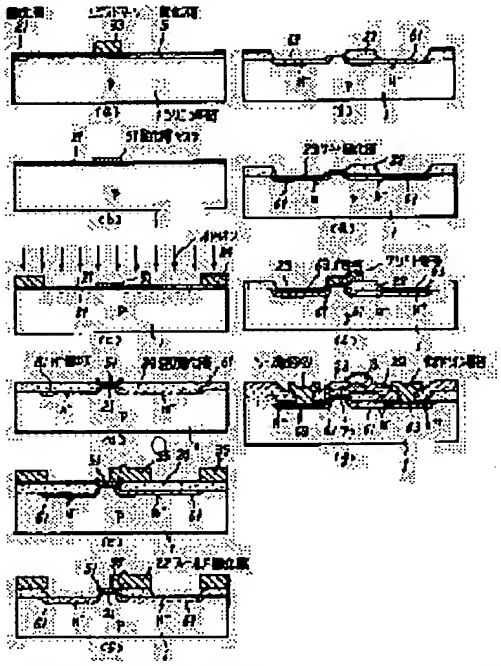
(54) MANUFACTURE OF MIS FIELD-EFFECT TRANSISTOR

(57)Abstract:
PURPOSE: To form a high-breakdown strength MISFET by a method wherein a low-concentration-impurity diffusion process and a selective oxidation process are performed simultaneously, and a field oxide film formed only in a drain part and a low-concentration-impurity region are formed in a self-aligned manner.
CONSTITUTION: An oxide film 21 is formed on the surface of a P-type substrate 1; a nitride film 5 is deposited on it; a resist mask 33 is formed; an etching operation is performed; a nitride-film mask 51 is formed. P ions are implanted into a part, to be used as a low-concentration-impurity region, from an opening part which is formed of the resist mask 33 and the nitride-film mask 51. Consequently, the nitride film and the implantation of the P ions are performed in a self-aligned manner. Then, a diffused region 61 and a selective oxide film 24 are formed by an oxidation and diffusion process. A resist mask 35 is formed; after that, the oxide film 24 in a source-drain electrode part is removed by an etching operation; a field oxide film 22 is left. Then, the oxide film 21 on the P-type substrate 1 is removed; after that, a gate oxide film 23 is formed; an Si layer is deposited on it; a gate electrode 7 is formed; after that, an N++ region 63 and source-drain electrodes 91, 92 are formed.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

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[Date of requesting appeal against examiner's decision of rejection]

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* NOTICES *

CLAIMS

[Claim(s)]
[Claim 1] The process which carries out an ion implantation to the field which sandwiches the nitride mask which formed the front face of the semi-conductor layer of the first electric conduction form a wrap process and on the oxide film with the oxide film, The oxidation diffusion process which makes the field by which the thick oxide film was grown up and the ion implantation was carried out on the oxide film of the part which is not covered with a nitride mask the low high-impurity-concentration field of the second electric conduction form, Remove said thick oxide film on the low high-impurity-concentration field by the side of [one] a nitride mask, and the source electrode contact section is formed. The process which leaves the part near the nitride mask of said thick oxide film on the low high-impurity-concentration field by the side of another side of a nitride mask, considers as field oxide, removes a far part, and forms the drain electrode contact section, The manufacture approach of the MIS mold field-effect transistor characterized by including the process which removes a nitride mask and forms a gate electrode through gate oxide after it.
[Claim 2] The front face of the semi-conductor layer of the first electric conduction form one by one with the first oxide film, a nitride, and the second oxide film A wrap process, The process which carries out an ion implantation to two fields of a semi-conductor layer alternatively through the three film, The process which removes alternatively the nitride on the part near another side of the field where the ion implantation of one side was carried out with the second oxide film on it, The oxidation diffusion process which makes the field by which field oxide was grown up and the ion implantation was carried out on the first oxide film exposed by removal of a nitride the low high-impurity-concentration field of the second electric conduction form, The manufacture approach of the MIS mold field-effect transistor characterized by including the process which forms a gate electrode through gate oxide on the part which removed the nitride with the second oxide film for a start [of the upper and lower sides], and was pinched by both the low high-impurity-concentration field.
[Claim 3] The manufacture approach of the MIS mold field-effect transistor according to claim 2 which forms the part which divides two fields of the mask for carrying out an ion implantation alternatively with polycrystalline silicon.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention is the MIS mold (Metal Insulator Semiconductor) field-effect transistor which made the channel side of a drain field low high impurity concentration for the raise in pressure-proofing. (it omits Following MISFET) It is related with the manufacture approach.
[0002]
[Description of the Prior Art] Current [MISFET] is used for many electronic circuitries. And for the raise in pressure-proofing of MISFET, a low high-impurity-concentration diffusion field is built to the channel side of a drain field, and the approach of easing the electric field of the drain section by field oxide is taken. Drawing 2 (a) - (e) The production process of the high proof pressure MISFET of the conventional field offset mold is shown. First, after forming the oxide film 21 with a thickness of 30nm in the front face of the P type silicon substrate 1, the donor ion 4 is injected into the part in which a source drain electrode is prepared using the mask 31 of the resist film which has an aperture [drawing 2 (a)]. Next, a mask 31 is exfoliated and the donor ion 4 is injected into the part which forms field oxide using the mask 51 of the nitride which has an aperture, and the mask 32 of the resist film [drawing 2 (b)]. The resist film 32 is exfoliated after this and it is N by 1100 degrees C and heating for 20 minutes. - Fields 61 and 62 are formed and the selective oxidation film 22 as field oxide is formed according to an oxidation process [drawing 2 (c)]. Therefore, the N type low high-impurity-concentration field 61 is formed in [the selective oxidation film 22] self align. Subsequently, polycrystalline silicon is deposited through gate oxide 23, and in order to carry out patterning etching, and to form the gate electrode 7 and to lower the contact resistance of a source drain electrode, the N++ field 63 is formed by high concentration impurity diffusion [drawing 2 (d)]. And after covering with an interlayer insulation film 8 and breaking a contact hole, the metal electrode 9 used as the source and a drain electrode is formed [drawing 2 (e)]. In addition, N - A field 62 is useful to electric-field relaxation of the high concentration impurity diffusion field 63.
[0003] Thus, to MISFET which gate oxide thin-film-ized, by taking low high-impurity-concentration drain structure and field offset structure, electric-field relaxation of the drain section was performed and drain pressure-proofing has improved.
[0004]
[Problem(s) to be Solved by the Invention] However, there are the following troubles in the manufacture approach of the above conventional high proof pressures MISFET. That is, in order to form the low concentration impurity diffusion field 61 in self align with the nitride 51 used as the mask for selective oxidation film 22 formation, to a drain junction periphery, electric-field relaxation becomes homogeneity. However, N - A field 61 has the fault that on resistance increases, in order that it may be formed also in the source section and resistance of the part may occupy 10% or more of the on resistance of a component.
[0005] On the other hand, although it is also possible to set without forming in the source section by forming a low concentration impurity diffusion field before a selective oxidation film formation process, and to reduce on resistance, electric-field relaxation of the drain section becomes uneven, and a result to which the dependability of a component is reduced is brought. The purpose of this invention is to offer the manufacture approach of MISFET which does not increase source resistance while it establishes a low high-impurity-concentration field in the bottom of the field oxide of the drain section and performs uniform electric-field relaxation except for an above-mentioned fault.
[0006]
[Means for Solving the Problem] In order to attain the above-mentioned purpose, the manufacture approach of MISFET of this invention The process which carries out an ion implantation to the field which sandwiches the nitride mask which formed the front face of the semi-conductor layer of the first electric conduction form a wrap process and on the oxide film with the oxide film, The oxidation diffusion process which makes the field by which the thick oxide film was grown up and the ion implantation was carried out on the oxide film of the part which is not covered with a nitride mask the low high-impurity-concentration field of the second electric conduction form, Remove said thick oxide film on the low high-impurity-concentration field by the side of [one] a nitride mask, and the source electrode contact section is formed. The process which leaves the part near the nitride mask of said thick oxide film on the low high-impurity-concentration field by the side of another side of a nitride mask, considers as field oxide, removes a far part, and forms the drain electrode contact section, A nitride mask shall be removed and the process which forms a gate electrode through gate oxide after it shall be included. The front face of the semi-conductor

layer of the first electric conduction form one by one with the first oxide film, a nitride, and the second oxide film Or a wrap process, The process which carries out an ion implantation to two fields of a semi-conductor layer alternatively through the three film, The process which removes alternatively the nitride on the part near another side of the field where the ion implantation of one side was carried out with the second oxide film on it, The oxidation diffusion process which makes the field by which field oxide was grown up and the ion implantation was carried out on the first oxide film exposed by removal of a nitride the low high-impurity-concentration field of the second electric conduction form, The process which forms a gate electrode through gate oxide on the part which removed the nitride with the second oxide film for a start [of the upper and lower sides], and was pinched by both the low high-impurity-concentration field shall be included. And it is effective to form the part which divides two fields of the mask for carrying out an ion implantation alternatively with polycrystalline silicon.

[0007]

[Function] After performing an ion implantation to two fields for low high-impurity-concentration field formation by using a nitride pattern as a mask, By forming a respectively thick oxide film on each field, removing all the thick oxide films on the other hand, breaking the source electrode contact surface, leaving field oxide on the other hand, and breaking the drain electrode contact surface Field oxide can be formed in the field which does not have a nitride after forming a low high-impurity-concentration field in self align with a nitride only at the drain section.

[0008] Or after performing the ion implantation which forms a low high-impurity-concentration field alternatively through the oxide film which sandwiches a nitride, by removing a part of nitride on one ion-implantation field, and forming field oxide in the part, field oxide is not formed in the source section, but field oxide is formed in the one side of the field which poured in ion in self align in the drain section. Since there is no field oxide in the source section in any case, there is no increase of the source resistance by the low high-impurity-concentration field under it.

[0009]

[Example] Drawing which gave the same sign to drawing 2 and a common part hereafter is quoted, and the example of this invention is described. drawing 1 (a) - (i) one shown example — the front face of p form substrate 1 — thickness 30nm an oxide film 21 — forming — further — a it top — 100nm in thickness a nitride 5 — depositing — the resist mask 33 — preparing — [drawing 1 R> 1 (a)] and [drawing 1 (b)] which etches and forms the nitride mask 51. Subsequently, they are acceleration voltage 50keV, and dose 1.0x1013 atom / cm2 to the part which builds a low high-impurity-concentration field from opening formed with the resist mask 34 and the nitride mask 51. **** (P) Ion 4 is poured in [drawing 1 (c)]. Therefore, impregnation of a nitride 51 and the P ion 4 is performed in self align. next, an oxidation diffusion process — a junction depth of 1.0 micrometers from the impregnation field of the P ion 4, surface high-impurity-concentration 2x1017 atom / cm3 N- 600nm in the diffusion field 61 and thickness [Drawing 1 (d)] which forms the selective oxidation film 24. Then, the resist mask 35 is formed on the selective oxidation film 24, [drawing 1 (e)] and etching remove the oxide film 24 of the source drain polar zone, and it leaves field oxide 22. Next, the resist mask 35, the nitride mask 51, and N - P inserted between fields 61 - The oxide film 21 on the exposure of a layer 1 is removed [drawing 1 (g)]. Then, exposed N - The N++ field 63 for forming gate oxide 23 with a thickness of 25nm on the field of a field 61, depositing and carrying out patterning of the polycrystalline silicon (Si) layer, and forming the gate electrode 7 [drawing 1 (h)] and on it, and lowering contact resistance with an electrode is formed [drawing 1 (i)]. Furthermore, after covering with an interlayer insulation film 8 and breaking a contact hole, the high proof pressure MISFET is done by forming the source electrode 91 and the drain electrode 92 with an aluminum-Si alloy etc. [drawing 1 (j)].

[0010] Drawing 3 (a) - (h) In the shown another example 100nm in thickness after forming the oxide film 21 with a thickness of 30nm on the P type silicon substrate 1 A nitride 5 is deposited. Furthermore the front face of the nitride 5 is oxidized, the oxide film 25 with a thickness of 10nm is formed, and the resist mask 36 is formed on it after depositing the polycrystal Si layer 10 with a thickness of 50nm on it [drawing 3 (a)]. And it etches using this mask and the polycrystal Si mask 11 is formed [drawing 3 (b)]. At this time, terminal point detection of etching with the oxide film 25 on a nitride 5 is possible. Acceleration voltage 50keV and the P ion 4 of a dose 1.0x1013 are injected into the part which builds a low high-impurity-concentration field from opening formed with the polycrystal Si mask 11 and the resist mask 34 next [drawing 3 (c)]. The resist mask 37 which carries out opening to the part which forms field oxide after it and on it is formed [drawing 3 (d)]. And an oxide film 25 and a nitride 5 are etched using the resist mask 37 and the polycrystal Si mask 11, and the resist film 37 is removed [drawing 3 (e)]. subsequently, an oxidation diffusion process — a junction depth of 1.0 micrometers from the impregnation field of the P ion 4, surface high-impurity-concentration 2x1017 atom / cm3 N- 600nm in the diffusion field 61 and thickness [Drawing 3 (f)] which removes the polycrystal Si mask 11, an oxide film 25, a nitride 5, and an oxide film 21, and forms gate oxide 23 with a thickness of 25nm after forming the selective oxidation film 22. Then, patterning of the polycrystal Si layer is deposited and carried out, and the gate electrode 7 is formed [drawing 3 (g)]. It is drawing 1 (i) to the last. And (j) The N++ field 63 for lowering contact resistance with an electrode is similarly formed with having been shown, and after covering with an interlayer insulation film 8 and breaking a contact hole, the source electrode 91 and the drain electrode 92 are formed [drawing 3 (h)].

[0011] Although each above-mentioned example described high proof-pressure N channel MISFET, it can be similarly carried out in high proof-pressure P channel MISFET. Moreover, the usual low proof pressure MISFET or the low proof pressure MISFET made detailed can be formed in the same semi-conductor substrate other than the high proof pressure MISFET shown in the example at coincidence.

[0012]

[Effect of the Invention] According to this invention, as stated above, by performing a low concentration impurity diffusion process to a selective oxidation process and coincidence, and forming the field oxide and the low high-impurity-concentration field which are established only in the drain section in self align, channel length was not influenced by alignment, but source resistance was low, the high proof pressure MISFET which has a low high-impurity-concentration field in the channel side of only the drain section was obtained, and contraction of the chip size of the high proof pressure MISFET and the improvement in dependability of him were attained.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is (a) about the production process of the high proof pressure MISFET of one example of this invention. Or (j) Sectional view shown in order
[Drawing 2] It is (a) about the production process of the conventional high proof pressure MISFET. Or (e) Sectional view shown in order
[Drawing 3] It is (a) about the production process of the high proof pressure MISFET of another example of this invention. Or (h) Sectional view shown in order
[Description of Notations]
1 P Type Silicon Substrate
21 Oxide Film
22 Field Oxide
23 Gate Oxide
24 Selective Oxidation Film
25 Oxide Film
33 Resist Mask
34 Resist Mask
35 Resist Mask
36 Resist Mask
37 Resist Mask
4 P Ion
5 Nitride
51 Nitride Mask
61 N - Field
63 N++ Field
7 Gate Electrode
91 Source Electrode
92 Drain Electrode
10 Polycrystalline Silicon Layer
11 Polycrystalline Silicon Mask

[Translation done.]

(19)日本国特許庁（ＪＰ）　(12) **公開特許公報（Ａ）**　(11)特許出願公開番号

特開平6－29525

(43)公開日　平成６年(1994)２月４日

(51)Int.Cl.[5]	識別記号	庁内整理番号	ＦＩ	技術表示箇所
Ｈ０１Ｌ　29/784				
21/336				
		7377－4M	Ｈ０１Ｌ　29/ 78	３０１　Ｓ
		7377－4M		３０１　Ｐ

審査請求　未請求　請求項の数３(全　５　頁)

(21)出願番号　特願平4－178713

(22)出願日　平成４年(1992)７月７日

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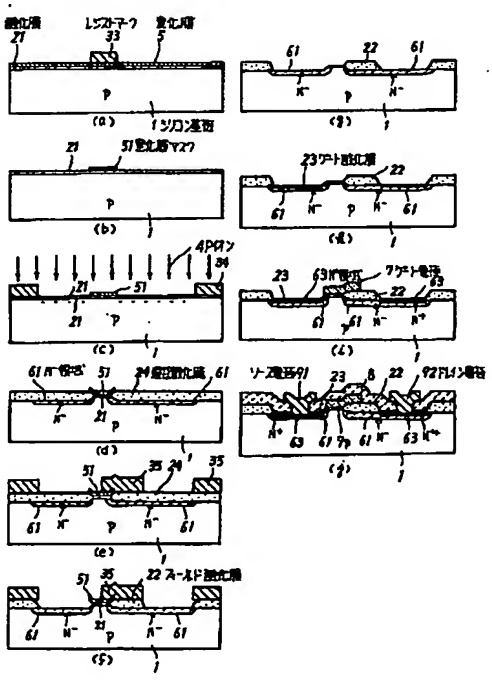
(54)【発明の名称】　ＭＩＳ型電界効果トランジスタの製造方法

(57)【要約】
【目的】ドレイン領域のチャネル側に低不純物濃度領域とその上のフィールド酸化膜を形成する高耐圧ＭＩＳＦＥＴのソース抵抗の増大を防止する。
【構成】窒化膜マスクをはさむ二つの領域にイオン注入し、その領域を低不純物濃度領域とすると共にその上に厚い酸化膜を形成し、ドレイン側ではその酸化膜からフィールド酸化膜を形成するが、ソース側ではその酸化膜を除去することによりソース抵抗の増大を防ぐ。あるいは、窒化膜を上下の酸化膜ではさみ、その３膜を通してイオン注入し、イオン注入領域を低不純物濃度にすると共に、そのドレイン側のみで窒化膜の一部を除去してその部分にフィールド酸化膜をつくることにより、ソース抵抗の増大を防ぐ。



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【特許請求の範囲】

【請求項１】第一導電形の半導体層の表面を酸化膜で覆う工程と、その酸化膜の上に形成した窒化膜マスクをはさむ領域にイオン注入する工程と、窒化膜マスクに覆われない部分の酸化膜上に厚い酸化膜を成長させ、またイオン注入された領域を第二導電形の低不純物濃度領域とする酸化拡散工程と、窒化膜マスクの一方の側の低不純物濃度領域上の前記厚い酸化膜を除去してソース電極接触部を形成し、窒化膜マスクの他方の側の低不純物濃度領域上の前記厚い酸化膜の窒化膜マスクに近い部分を残してフィールド酸化膜とし、遠い部分を除去してドレイン電極接触部を形成する工程と、窒化膜マスクを除去し、そのあとにゲート酸化膜を介してゲート電極を形成する工程とを含むことを特徴とするＭＩＳ型電界効果トランジスタの製造方法。

【請求項２】第一導電形の半導体層の表面を第一酸化膜、窒化膜および第二酸化膜で順次覆う工程と、その３膜を通して選択的に半導体層の二つの領域にイオン注入する工程と、一方のイオン注入された領域の他方に近い部分上の窒化膜をその上の第二酸化膜と共に選択的に除去する工程と、窒化膜の除去によって露出した第一酸化膜上にフィールド酸化膜を成長させ、またイオン注入された領域を第二導電形の低不純物濃度領域とする酸化拡散工程と、窒化膜をその上下の第一、第二酸化膜と共に除去して両低不純物濃度領域にはさまれた部分の上にゲート酸化膜を介してゲート電極を形成する工程とを含むことを特徴とするＭＩＳ型電界効果トランジスタの製造方法。

【請求項３】選択的にイオン注入するためのマスクの二つの領域を分割する部分を多結晶シリコンで形成する請求項２記載のＭＩＳ型電界効果トランジスタの製造方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、高耐圧化のためにドレイン領域のチャネル側を低不純物濃度にしたＭＩＳ (Metal Insulator Semiconductor)型電界効果トランジスタ(以下ＭＩＳＦＥＴと略す）の製造方法に関する。

【０００２】

【従来の技術】現在ＭＩＳＦＥＴは多くの電子回路に用いられている。そして、ＭＩＳＦＥＴの高耐圧化のため、ドレイン領域のチャネル側に低不純物濃度拡散領域をつくり、フィールド酸化膜によるドレイン部の電界を緩和する方法がとられている。図２(a) ～(e) は、従来のフィールドオフセット型の高耐圧ＭＩＳＦＥＴの製造工程を示す。まず、Ｐ型シリコン基板１の表面に30nmの厚さの酸化膜21を形成したのち、ソース・ドレイン電極の設けられる部分に窓を有するレジスト膜のマスク31を用いてドナーイオン４を注入する〔図２(a) 〕。次に、マスク31を剥離し、フィールド酸化膜を形成する部分に

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窓を有する窒化膜のマスク51とレジスト膜のマスク32を用いてドナーイオン４を注入する〔図２(b) 〕。このあとレジスト膜32を剥離し、1100℃、20分の加熱でN^- 領域61および62を形成し、また酸化工程によりフィールド酸化膜としての選択酸化膜22を形成する〔図２(c) 〕。従ってＮ形低不純物濃度領域61は選択酸化膜22とは自己整合的に形成される。次いで、ゲート酸化膜23を介して多結晶シリコンを堆積し、パターニングエッチングしてゲート電極７を形成し、また、ソース・ドレイン電極の接触抵抗を下げるため高濃度不純物拡散によりN^{++}領域63を形成する〔図２(d) 〕。そして、層間絶縁膜８で被覆し、接触孔を明けたのち、ソースおよびドレイン電極となる金属電極９を形成する〔図２(e) 〕。なお、N^-領域62は高濃度不純物拡散領域63の電界緩和用に役立つ。

【０００３】このように、ゲート酸化膜が薄膜化したＭＩＳＦＥＴに対し、低不純物濃度ドレイン構造とフィールドオフセット構造をとることにより、ドレイン部の電界緩和が行われ、ドレイン耐圧が向上してきた。

【０００４】

【発明が解決しようとする課題】しかしながら、上記のような従来の高耐圧ＭＩＳＦＥＴの製造方法には次のような問題点がある。すなわち、低濃度不純物拡散領域61を選択酸化膜22形成のためのマスクとなる窒化膜51と自己整合的に形成するため、ドレイン接合周辺部に対しては電界緩和が均一になる。しかし、N^- 領域61はソース部にも形成されその部分の抵抗が素子のオン抵抗の10%以上を占めるため、オン抵抗が増大するという欠点がある。

【０００５】これに対し、低濃度不純物拡散領域を選択酸化膜形成工程の前に形成することによりソース部に形成しないでおき、オン抵抗を低減することも可能であるが、ドレイン部の電界緩和が不均一となり、素子の信頼性を低下させる結果となる。本発明の目的は、上述の欠点を除き、ドレイン部のフィールド酸化膜の下に低不純物濃度領域を設けて均一な電界緩和を行うと共に、ソース抵抗を増大させることのないＭＩＳＦＥＴの製造方法を提供することにある。

【０００６】

【課題を解決するための手段】上記の目的を達成するために、本発明のＭＩＳＦＥＴの製造方法は、第一導電形の半導体層の表面を酸化膜で覆う工程と、その酸化膜の上に形成した窒化膜マスクをはさむ領域にイオン注入する工程と、窒化膜マスクに覆われない部分の酸化膜上に厚い酸化膜を成長させ、またイオン注入された領域を第二導電形の低不純物濃度領域とする酸化拡散工程と、窒化膜マスクの一方の側の低不純物濃度領域上の前記厚い酸化膜を除去してソース電極接触部を形成し、窒化膜マスクの他方の側の低不純物濃度領域上の前記厚い酸化膜の窒化膜マスクに近い部分を残してフィールド酸化膜と

し、遠い部分を除去してドレイン電極接触部を形成する工程と、窒化膜マスクを除去し、そのあとにゲート酸化膜を介してゲート電極を形成する工程とを含むものとする。あるいは、第一導電形の半導体層の表面を第一酸化膜、窒化膜および第二酸化膜で順次覆う工程と、その３膜を通して選択的に半導体層の二つの領域にイオン注入する工程と、一方のイオン注入された領域の他方に近い部分上の窒化膜をその上の第二酸化膜と共に選択的に除去する工程と、窒化膜の除去によって露出した第一酸化膜上にフィールド酸化膜を成長させ、またイオン注入された領域を第二導電形の低不純物濃度領域とする酸化拡散工程と、窒化膜をその上下の第一、第二酸化膜と共に除去して両低不純物濃度領域にはさまれた部分の上にゲート酸化膜を介してゲート電極を形成する工程とを含むものとする。そして、選択的にイオン注入するためのマスクの二つの領域を分割する部分を多結晶シリコンで形成することが有効である。

【０００７】

【作用】窒化膜パターンをマスクとして低不純物濃度領域形成のための二つの領域にイオン注入を行ったのち、それぞれの領域の上にそれぞれ厚い酸化膜を形成し、一方ではその厚い酸化膜全部を除去してソース電極接触面を明け、他方ではフィールド酸化膜を残してドレイン電極接触面を明けることにより、低不純物濃度領域を窒化膜と自己整合的に形成した上で窒化膜のない領域にフィールド酸化膜をドレイン部のみに形成できる。

【０００８】あるいは、低不純物濃度領域を選択的に形成するイオン注入を窒化膜をはさむ酸化膜を通して行ったのち、一方のイオン注入領域上の窒化膜を一部除去してその部分にフィールド酸化膜を形成することにより、ソース部にはフィールド酸化膜は形成されず、ドレイン部ではフィールド酸化膜がイオンを注入した領域の一方側に自己整合的に形成される。いずれの場合もソース部にフィールド酸化膜がないので、その下の低不純物濃度領域によるソース抵抗の増大がない。

【０００９】

【実施例】以下、図２と共通の部分に同一の符号を付した図を引用して本発明の実施例について述べる。図１(a)～(i)に示した一実施例では、ｐ形基板１の表面に厚さ 30nm の酸化膜21を形成し、さらにその上に厚さ100nm の窒化膜５を堆積し、レジストマスク33を設け〔図１(a)〕、エッチングして窒化膜マスク51を形成する〔図１(b)〕。次いで、レジストマスク34と窒化膜マスク51により形成された開口部から低不純物濃度領域をつくる部分に加速電圧50keV 、ドーズ量1.0×10^{13}原子／cm^2 でりん(P) イオン４を注入する〔図１(c)〕。従って、窒化膜51とＰイオン４の注入は自己整合的に行われる。次に酸化拡散工程により、Ｐイオン４の注入領域から接合深さ1.0μm、表面不純物濃度２×10^{17}原子／cm^3 のN⁻ 拡散領域61および厚さ600nm の選択酸化膜24を

形成する〔図１(d)〕。このあと、選択酸化膜24の上にレジストマスク35を形成し〔図１(e)〕、エッチングによりソース・ドレイン電極部の酸化膜24を除去し、フィールド酸化膜22を残す。次に、レジストマスク35、窒化膜マスク51およびN⁻ 領域61の間にはさまれたP⁻ 層１の露出面上の酸化膜21を除去する〔図１(g)〕。その後、露出したN⁻ 領域61の面上に厚さ25nmのゲート酸化膜23を形成し〔図１(h)〕、その上に多結晶シリコン(Si)層を堆積し、パターニングしてゲート電極７を形成し、また電極との接触抵抗を下げるためのN⁺⁺領域63を形成する〔図１(i)〕。さらに、層間絶縁膜８で被覆し、接触孔を明けたのち、ソース電極91、ドレイン電極92をAl－Si合金等で形成することにより、高耐圧ＭＩＳＦＥＴができ上がる〔図１(j)〕。

【００１０】図３(a)～(h)に示す別の実施例では、Ｐ形シリコン基板１の上に厚さ30nmの酸化膜21を形成後、厚さ100nm の窒化膜５を堆積し、さらにその窒化膜５の表面を酸化して厚さ10nmの酸化膜25を形成し、その上に厚さ50nmの多結晶Si層10を堆積後、その上にレジストマスク36を設ける〔図３(a)〕。そしてこのマスクを用いてエッチングし、多結晶Siマスク11を形成する〔図３(b)〕。このとき、窒化膜５の上の酸化膜25によりエッチングの終点検出が可能である。つぎに、多結晶Siマスク11とレジストマスク34によって形成された開口部から低不純物濃度領域をつくる部分に加速電圧50keV 、ドーズ量1.0×10^{13}のＰイオン４の注入を行う〔図３(c)〕。そのあと、その上にフィールド酸化膜を形成する部分に開口するレジストマスク37を設ける〔図３(d)〕。そして、レジストマスク37と多結晶Siマスク11を用いて酸化膜25と窒化膜５をエッチングし、レジスト膜37を除去する〔図３(e)〕。次いで、酸化拡散工程により、Ｐイオン４の注入領域から接合深さ1.0μm、表面不純物濃度２×10^{17}原子／cm^3 のN⁻ 拡散領域61および厚さ600nm の選択酸化膜22を形成したのち、多結晶Siマスク11、酸化膜25、窒化膜５、酸化膜21を除去し、厚さ25nmのゲート酸化膜23を形成する〔図３(f)〕。このあと、多結晶Si層を堆積し、パターニングしてゲート電極７を形成する〔図３(g)〕。最後に図１(i)および(j)に示したと同様に、電極との接触抵抗を下げるためのN⁺⁺領域63を形成し、層間絶縁膜８で被覆し、接触孔を明けたのち、ソース電極91、ドレイン電極92を形成する〔図３(h)〕。

【００１１】上記の実施例はいずれも高耐圧Ｎチャネル ＭＩＳＦＥＴについて述べたが、高耐圧Ｐチャネル ＭＩＳＦＥＴにおいても同様に実施できる。また、実施例に示した高耐圧ＭＩＳＦＥＴのほかに、通常の低耐圧ＭＩＳＦＥＴあるいは微細化した低耐圧ＭＩＳＦＥＴも同一半導体基板に同時に形成できる。

【００１２】

【発明の効果】以上述べたように、本発明によれば、低

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濃度不純物拡散工程を選択酸化工程と同時に行い、ドレイン部にのみ設けられるフィールド酸化膜と低不純物濃度領域を自己整合的に形成することにより、チャネル長がアライメントに左右されず、ソース抵抗が低く、ドレイン部のみのチャネル側に低不純物濃度領域を有する高耐圧ＭＩＳＦＥＴが得られ、高耐圧ＭＩＳＦＥＴのチップサイズの縮小、信頼性向上が可能となった。

【図面の簡単な説明】

【図１】本発明の一実施例の高耐圧ＭＩＳＦＥＴの製造工程を(a) ないし(j) の順に示す断面図

【図２】従来の高耐圧ＭＩＳＦＥＴの製造工程を(a) ないし(e) の順に示す断面図

【図３】本発明の別の実施例の高耐圧ＭＩＳＦＥＴの製造工程を(a) ないし(h) の順に示す断面図

【符号の説明】

1　Ｐ形シリコン基板
21　酸化膜
22　フィールド酸化膜
＊23　ゲート酸化膜
24　選択酸化膜
25　酸化膜
33　レジストマスク
34　レジストマスク
35　レジストマスク
36　レジストマスク
37　レジストマスク
4　Ｐイオン
5　窒化膜
51　窒化膜マスク
61　N^- 領域
63　N^{++}領域
7　ゲート電極
91　ソース電極
92　ドレイン電極
10　多結晶シリコン層
＊11　多結晶シリコンマスク

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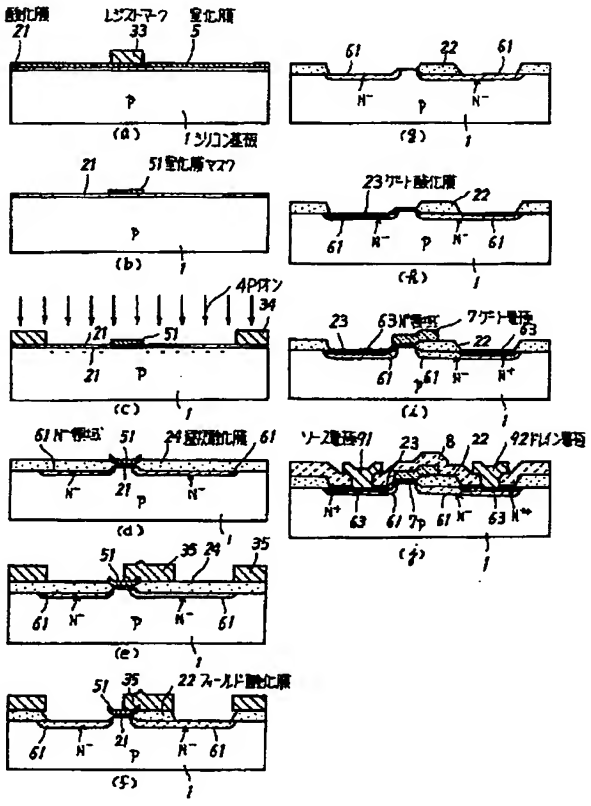
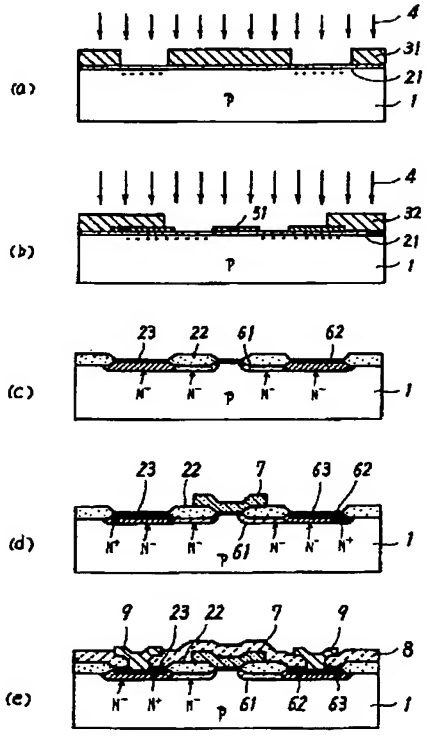
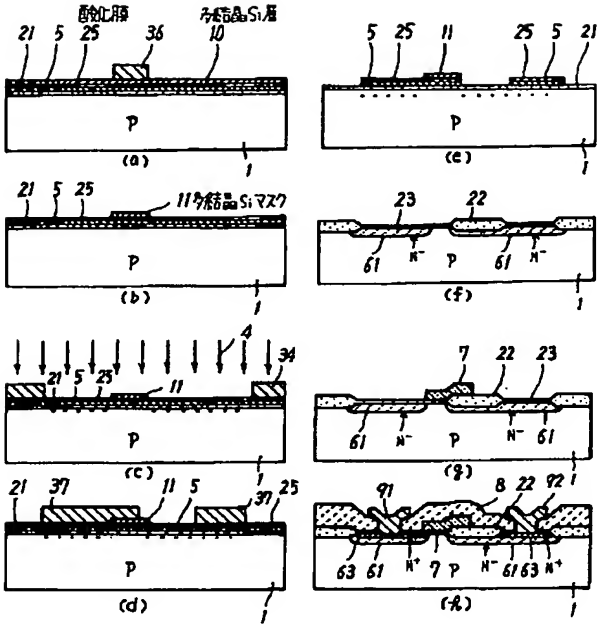
【図１】



【図２】



【図3】


酸化膜
多結晶Si層
21 5 25 36 10
P
(a)
1
21 5 25 11 多結晶Siマスク
(b)
4 34
11
(c)
21 37 11 5 37 25
(d)
5 25 11 25 5 21
(e)
23 22
61 N⁻ P 61 N⁻
(f)
7 22 23
(g)
91 8 22 92
63 61 N⁺ 7 P N⁻ 61 63 N⁺
(h)